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Applicant:	**Martin A. Cotton**	**Group Art: Unknown**
Application No.:	**Not Yet Assigned**	**Examiner: Unknown**
Filed:	**Herewith**	

For: NON-CIRCULAR MICRO-VIA

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

List of Sections Forming Part of This Information Disclosure Statement

The following sections are being submitted for this Information Disclosure Statement:

1. [X] Preliminary Statements
2. [X] Form PTO-1449 (Modified)
3. [ ] Statement as to Information Not Found in Patents or Publications
4. [ ] Identification of Prior Application in Which Listed Information Was Already Cited and for Which No Copies Are Submitted or Need Be Submitted
5. [ ] Cumulative Patents or Publications
6. [ ] Copies of Listed Information Items Accompanying this Statement

7. [ ] Concise Explanation of Non-English Language Listed Information Items

7A. [ ] EPO Search Report

7B. [ ] English Language Version

8. [ ] Translation(s) of Non-English Language Documents

9. [ ] Concise Explanation of English Language Listed Information Items (Optional)

10. [X] Identification of Person(s) Making this Information Disclosure Statement

Section 1. Preliminary Statements

Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 C.F.R. § 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability or that no other material information exists.

The filing of this information disclosure statement shall not be construed as an admission against interest in any manner. Notice of January 9, 1992, 1135 O.G. 13-25, at 25.

Section 2. Form PTO-1449 (Modified)

[X] A Completed Form PTO-1449 (Modified) is attached hereto.

Section 3. Statement as to Information Not Found in Patents or Publications (Information Not Listed in Form PTO-1449(Modified))

This invention relates to Printed Circuit Boards (PCBs) and particularly to micro-via plated through hole interconnect and shielding structures for PCBs and the method for creating such micro-vias and shielding structures.

It is always the goal in PCB design to increase the functionality and component capacity. Almost since the inception of PCB's, engineers have striven to add more and more functionality and hence more interconnect traces. These traces go from side to side and from layer to layer and in this way form the interconnect between the"active"electronic elements. The PCB has throughout its lifetime been made from many alternate materials and processes. The most common material being a glass epoxy based laminate, with the PCB builds being of a single sided, double sided or a multilayered (more than 2 layers) configuration. The interconnect medium between layers are created by drilling with mechanical drill through the layers of the PCB exposing the copper interconnect lands on the individual layers. The PCB is then passed through a plating solution and the various layers are connected by plated or deposited copper formed on the interior surface of the drilled through hole. This drilled plated barrel of inter layer interconnect is called a "via". The most obvious physical attribute is that the via is round when viewed from the top or bottom side. This is caused by"drilling". Drilling holes through laminate causes a round or circular hole to be created. Drilling of holes is carried out on a drilling machine that drills using a"drill", a mechanical device that rotates or cuts around its centerline cutting away material about the centerline to create the round or circular holes. The action of a drill is one of cutting.

As mentioned previously more and more interconnect traces have been required as circuit and hence PCB complexity increased. This of course has led to a decrease in size of the vias and an increase in their number. The new smaller vias are called"micro vias"and are typically of a blind nature. Blind vias are vias that do not pass completely through the PCB, but stop at some predetermined layer depth. The smaller via size is required due to an increase in trace density which reduces the points on a given layer where a terminal interconnect land can be positioned such that it aligns with a land on another layer without interference with traces there between. If cross-sectional real estate that a via occupies is reduced, the ability to utilize a via is more likely.

However, the decrease in via size has meant that the mechanical drilling of micro vias is almost commercially extinct. Several alternate processes have sprung up namely laser ablation and plasma ablation. Material ablation is an electrochemical reaction to either laser light pulsing or the plasma process. It is not a cutting action or process. However, ablation in like manner removes away material around a centerline.

Ablation emulates mechanical drilling by creating a basically circular hole whichever method is used. This ablated round hole is often described as "drilling"because of removal of material about a centerline, hence the term, Micro via drilling. This round hole has performance level based around the creation of a round or circular shape hole, namely, current carrying capacity, resistance and inductance. For example, a blind via has a lower inductance than a through hole because it has shorter length to the barrel of the via, but its current carrying capacity does not alter because the diameter and hence the circumference of the hole remains the same. Therefore, the current carrying capacity of

a via is dependent on the circumferencial length and the conducting medium thickness at the point of interconnection between the trace land and the via.

There are several problems with the conventional circular profile micro- via. For example, when densely populated multi-layer PCBs are utilized there are an enormous amount of traces and interconnects. Circular vias may be a limiting feature if the via is to avoid traces or components when extending through multiple layers because of the cutting area required for a circular hole.

Also, the current carrying capacity of circular vias are limited because current carrying capacity of a via is a factor of circumference and thickness of the plating applied to the inner wall. This factor also effects the ability to have multiple traces on a single layer to connect up to the same via because the distance between the contact points are too short thus exceeding the current carrying capacity of the via at those points or the interconnect density at a given land or PCB layer. Conventional standard circular profile micro vias also have a characteristic inductance property due to the spiral nature of the circular via which effects the electron flow through the via resulting in an inductance. The inductance characteristic tends to slow down signal speed and increase noise susceptibility.

Through holes that can possibly be categorized as a Micro-via have been utilized on non-organic silicone based semi-conductor devices to connect two conductive layers separated by an insulation layer where the insulation layer has a contact through hole which exposes a portion of the two conductive surfaces. This through hole embodiment is where one conductive layer continuously extends down through the through-hole thereby electrically connecting the two layers. The semi-conductor via technology has a different purpose and hence a different structure, however it is worth mentioning when discussing via technology (electrical interconnection utilizing a through hole) for completeness. With a semiconductor via the first conductive layer actually conforms to the walls of the through hole and continues over the exposed area of the second layer and in continuous contact with said second layer forming what may be described as a blind via. However the process of forming the via is different from a process where material is cut away about a centerline and there is no plating structure.

In this semi-conductor example the through-hole is filled with a continuation of a first conductive layer of the semi-conductor into the through hole. The through hole structure utilized for semiconductor designs differs from through holes or micro vias utilized for printed circuit boards. First, micro vias for printed circuit boards interconnect a plurality of circuit trace terminal lands or pads by transcending through and exposing them to an interior conductive plating, whereas the semiconductor through hole structure is that of a hole through an insulation layer that separates two layers of conductive media. The interconnection is established by continuously extending one conductive media layer through the through hole establishing contact with the second layer. Establishing a plurality of interconnections to a node created by a via is not the objective in the semiconductor environment as it is with printed circuit board vias.

The specific issue with regard to semi conductor vias is electrical failure of the via structure due to thermal and other stresses particularly in the area around the rim of the opening of the through hole. This is where the conductive media layer begins to extend through the through hole and failures occur because it is at this point that the media layer tends to be thinner. The problem is concentration of stresses in a small area. Whereas, with printed circuit boards the issue with vias is the density of the interconnections as it relates to current carrying capacity and better voltage drop.

Section 4. Identification of Prior Application in Which Listed Information Was Already Cited and for Which No Copies Are Submitted or Need Be Submitted

This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application Serial No. 09/786,787, filed on May 10, 2001.

(complete the following, if applicable)

[ ] This application also relies, under 35 U.S.C. 120, on the earlier filing date of prior application Serial No. _____, filed on _____ (date).

The following references were submitted to, and/or cited by, the Office in the prior application(s) and therefore, are not required to be provided in this application:

Section 5. Cumulative Patents or Publications

STATEMENT

_____ is cumulative of the following patents or publications listed on Form PTO-1449:

In accordance with 37 C.F.R. § 1.98(c), a copy of only ____ is being submitted with this Information Disclosure Statement.

Section 6. Copies of Listed Information Items Accompanying this Statement

Legible copies of all items listed in Form PTO-1449 (Modified) accompany this information disclosure statement.

[ ] Exception(s) to above:

[ ] Items in prior application from which an earlier filing date is claimed for this application, as identified in Section 4.

[ ] Cumulative patents or publications identified in Section 5.

Section 7. Concise Explanation of Non-English Language Listed Information Items

Section 7A. Concise Explanation of Non-English Language Listed Information Items - EPO Search Report

The relevance with respect to the following citations listed on Form PTO-1449:

is submitted on the basis of accompanying:

(check the appropriate item)

[ ] EPO search report that is in the English language,

[ ] EPO search report that is not in the English language and that is accompanied also by an English language version of the EPO search report,

that issued on the corresponding European patent application.

Section 7B. Concise Explanation of Non-English Language Listed Information Items - English Language Version of EPO Search Report

Section 8. Translation(s) of Non-English Language Documents

[ ] Submitted herewith is an English translation of the following foreign language patents, publications or information or of those portions of those patents, publications or information considered to be material:

(complete the following, if applicable)

[ ] No English language translations of the foreign language parents, publications or information or parts thereof are readily available, except for those listed above.

[ ] The following foreign language documents submitted are believed to be the equivalent or substantial equivalent of the English language documents identified below, which are also submitted herewith.

Section 9. Concise Explanation of English Language Listed Information Items (OPTIONAL)

Section 10. Identification of Person(s) Making this INFORMATION DISCLOSURE STATEMENT

The person making this statement is the attorney who signs below on the basis of the information:

[ ] supplied by the inventor(s)

[ ] supplied by an individual associated with the filing and prosecution of this application (37 C.F.R. § 1.56(c)).

[X] in the attorney's file

Respectfully submitted,

Marc Brockhaus

Marc A. Brockhaus, Reg. No. 40,923
DUNLAP, CODDING & ROGERS, P.C.
P.O. Box 16370
Oklahoma City, Oklahoma 73113
(405) 607-8600 - telephone
(405) 607-8686 - telefax

Attorney for Applicants

Express Mail: EV33286755US
Date Deposited: October 30, 2003

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	Not Yet Assigned
Filing Date	Herewith
First Named Inventor	Martin A. Cotton
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	8245.061

U. S. PATENT DOCUMENTS

EXAM INIT.	Cite No. 1	U.S. PATENT NUMBER Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	5,270,493		Inoue, et al.	12-14-1993	
	AB	5,590,460		DiStefano, et al.	01-07-1997	
	AB	5,677,515		Selk, et al.	10-14-1997	
	AC	5,966,294		Harada, et al.	10-12-1999	
	AD	6,000,120		Arledge, et al.	12-14-1999	
	AE	6,388,208		Kiani, et al.	05-14-2002	

FOREIGN PATENT DOCUMENTS

EXAM INIT.	Cite No. 1	Foreign Patent Document: Office 3	Foreign Patent Document: Number 4	Foreign Patent Document: Kind Code5 (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

U.S. and Foreign: [1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). [4] Form Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard St. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

EXAM INIT.		NON PATENT DOCUMENTS
		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published

Non Patent Documents: [1] Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature: Date Considered:

EXAMINER: Initial if citation considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant. **Place of Publication refers to name of publication in which the information was published.